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D. Remarks

Objections to Claims.

Claims 25 to 29 have been renumbered to address the claim objections.

Rejection of Claims 1-3, 5-7, 21, and 23-24 Under 35 U.S.C. §102(e) based on *Uehara et al.* (USP 6,573,132).

The rejection of claims 1-3 and 5-7 will first be addressed.

The semiconductor device of amended claim 1 includes an insulated gate field effect transistor (IGFET). A gate electrode of the IGFET includes a lower layer electrode formed on a gate insulating film and an upper layer electrode formed on the lower layer electrode. A cap film is formed on the upper layer electrode. A first nitride film is on a side surface of the upper layer electrode. The first nitride film has a film thickness of approximately 2 to 5 nm. The IGFET includes an oxide film on a side surface of the lower electrode and an etching stopper film including a second nitride film formed on the outside of the first nitride film and oxide film.

As is well known, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference.

Claim 1 has been amended to include the limitations of claim 4. It is admitted that the cited reference does not include the limitations of claim 4:

> Regarding claims 4, 22 Uehara does not disclose the semiconductor device wherein the first nitride film 32 has a thickness of approximately 2-5 nm (Office Action, dated 8/25/04, Page 6, Section 7, Paragraph 2).

Accordingly, because the reference *Uehara et al.* does not show all elements of amended claim 1, this ground of rejection is traversed.

The rejection of claims 21, 23, and 24 will now be addressed.

The semiconductor device of amended claim 21 includes a first transistor formed in a first region. The first transistor includes a first upper layer gate electrode formed on and in electrical connection with a first corresponding lower layer gate electrode. A first insulating film formed on a side surface of the first lower layer gate electrode and not on the side surface of the first upper layer gate electrode. A second insulating film formed on a side surface of the first upper

layer gate electrode. The second insulating film having a lower thermal growth rate with respect to the first upper layer gate electrode material than the thermal growth rate of the first insulating film with respect to the first lower layer gate electrode material. A first etching stopper is formed on the outside of the first and second insulating films. The second insulating film has a thickness of less than 6 nm.

To address this rejection, the same essential arguments set forth above with respect to claim 1 are incorporated herein by reference. Namely, claim 21 has been amended to incorporate the limitations of claim 22. As shown by above Office Action excerpt, the cited reference *Uehara et al.* does not disclose the particular nitride thickness recited in amended claim 21.

Because the reference *Uehara et al.* does not show all elements of amended claim 21, this ground of rejection is also traversed.

Rejection of Claims 21 and 25-27 Under 35 U.S.C. §102(e) based on *Ota et al.* (USP 6,521,963).

The semiconductor device of amended claim 21 includes a first transistor formed in a first region. The first transistor includes a first upper layer gate electrode formed on and in electrical connection with a first corresponding lower layer gate electrode. A first insulating film formed on a side surface of the first lower layer gate electrode and not on the side surface of the first upper layer gate electrode. A second insulating film formed on a side surface of the first upper layer gate electrode. The second insulating film having a lower thermal growth rate with respect to the first upper layer gate electrode material than the thermal growth rate of the first insulating film with respect to the first lower layer gate electrode material. A first etching stopper is formed on the outside of the first and second insulating films. The second insulating film has a thickness of less than 6 nm.

FIG. 25 *Ota et al.* discloses a transistor that includes a polysilicon layer **4C**, tungsten nitride layer **51B**, and a tungsten layer **50B**. A silicon oxide film **14** is formed on the side of the polysilicon layer **4C** and a silicon nitride film **25B** (argued to correspond to applicant's second insulating film[1]) is formed on the side of the tungsten nitride layer **51B** and the tungsten layer **50B**.

However, *Ota et al.* does not disclose a second insulating film having a thickness of less than 6 nm as required by amended claim 21. *Ota et al.* is silent as to the thickness of silicon

[1] See the Office Action, dated 08/25/04, Page 4, Lines 14-15.

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nitride film 25B.[2]

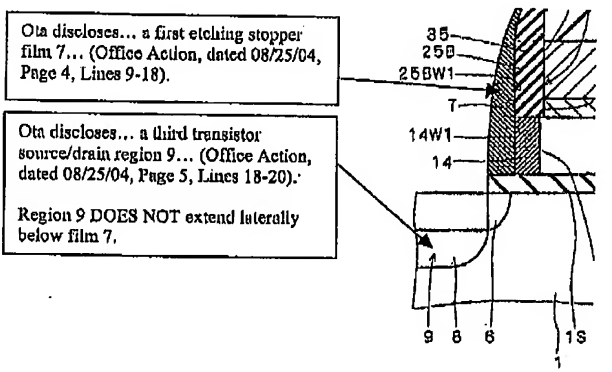
Thus, because the reference *Ota et al.* does not show all elements of amended claim 21, this ground of rejection is traversed.

Claim 27 (as renumbered by amendment) is believed to be separately patentable over *Ota et al.*

Claim 27, which depends from claim 26, recites a third transistor source/drain region having a different concentration than either the first or second transistor source/drain regions extending laterally below the first etching stopper film.

Claim 27 includes a third transistor source/drain region having a different concentration than either the first or second transistor source/drain regions extending laterally below the first etching stopper film.

The rejection of claim 27 identifies transistor source/drain region 9 of FIG. 26 as the third transistor source/drain region.[3] However, as shown in the below portion of FIG. 25 FROM *Ota et al.*, transistor source/drain region 9 is not "extending laterally below the first etching stopper film" as recited in claim 27:



Thus, because *Ota et al.* does not show a third transistor source/drain region having a different concentration than either the first or second transistor source/drain regions extending

[2] A detailed review of *Ota et al.* shows that no thickness value is ever attributed to silicon nitride film 25B or the resulting protective film 35 formed from etching film 25B.
[3] See page 5, last paragraph of Office Action dated August 26, 2004.

laterally below the first etching stopper film as recited in amended claim 27, claim 27 is believed to be separately patentable over *Ota et al.*

Rejection of Claims 4 and 22 Under 35 U.S.C. §103(a), based on *Uehara et al.*

The rejection of claim 4 will first be addressed.

Claim 1 has been amended to include the limitations of claim 4, and claim 4 has been cancelled. Thus, as amended, claim 1 includes the first nitride film has a film thickness of approximately 2 to 5 nm.

As is well known, in proceedings before the Patent and Trademark Office, the examiner bears the burden of establishing a prima facie case of obviousness based on the prior art.[4] In addition, to establish a prima facie case of obviousness, a rejection must meet three basic criteria. First, there must be some suggestion or motivation to modify a reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference(s) must teach or suggest all claim limitations.[5]

As noted above, the rejection notes that *Uehara et al.* does not show a first nitride film with the recited thickness. To show such a limitations, the rejection argues that a first nitride film thickness is obvious:

> Uehara discloses the nitride layer 32 has a thickness of about 10 nm... it would have been obvious... to use thickness teaching of *Uehara* in the range as claimed because it has been held that where the general conditions of the claims are disclosed in the prior art, it is not inventive to discover the optimum or workable range by routine examination. (Office Action, dated 08/25/04, Page 6, Section 7).

Applicant acknowledges the above rationale, but notes it has not been properly applied. In order for the optimization of a variable to be obvious, the variable must first be recognized as a result-effective variable.[6] That is, only after it has been demonstrated that the art recognizes the result effective variable, can the optimization of such a variable be considered obvious.

The rejection has provided no reason or rationale as to why the thickness of nitride layer 32 of *Uehara et al.* can be considered a result-effective variable. For this reason alone, the

[4] Ex parte Obukowicz, 27 USPQ 1063, 105 (B.P.A.I. 1992).
[5] MPEP §2143.
[6] MPEP §2144.05, II, B.

rejection is defective, and cannot have met the necessary burden of proof.

Second, nothing in cited art indicates that the thickness of nitride layer 32 is a result effective variable for any related purposes of the reference. Accordingly, the necessary factual support for a prima facie case of obviousness is not on record. Applicant notes that the reference appears to teach away from the proposed optimization. The nitride layer 32 is clearly an etch protective layer intended to maintain a protective etch selectivity. Thus, making this layer thinner would make is less suitable for its intended purpose (not optimal).

> In such a structure, even if the second nitride sidewall 33 and the insulator cap 31 are exposed within a contact hole being etched to form the contact 40, the etch selectivity of the second nitride sidewall 33 does not decrease. This is because the first nitride sidewall 32 is located under the upper edge portion of the second nitride sidewall 33. (*Uehara et al*, Col. 7, Lines 31-40).

If the examiner is taking official notice regarding this fact, Applicant seasonably traverses any such assertion and respectfully requests the citation in support. Applicant notes, such a citation should indicate why the thinness of nitride layer 32 would be considered a result effective variable.

For all of these reasons, the rejection has not established a prima facie case of obviousness for amended claim 1, and this ground for rejection is traversed.

The rejection of claim 22 will now be addressed.

Claim 21 has been amended to include the thickness limitations of claim 22. Thus, amended claim 21 recites that the second insulating film has a thickness of less than 6 nm.

To address this rejection, the same general arguments set forth above for claim 1 (as amended to include the limitations of claim 4). Namely, the rejection has not indicated how or why the thickness of nitride layer 32 is a result effective variable.

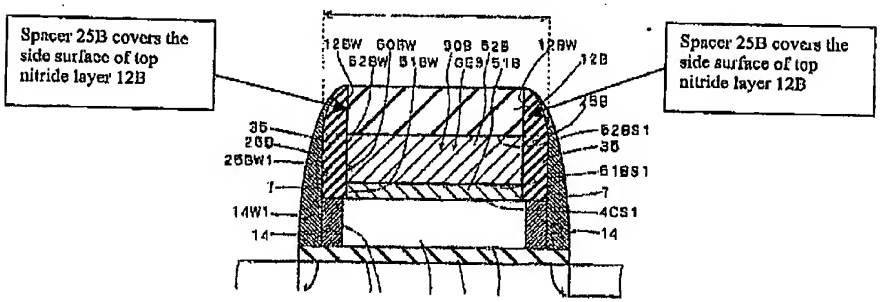
Further, as in the case of claim 1, if the examiner is taking official notice with respect to the thinness of the nitride layer in structure or *Uehara et al.*, Applicant seasonably traverses any such assertion and respectfully requests the citation in support.

For all of these reasons, a prima facie case of obviousness has not been established for amended claim 21, and this ground for rejection is traversed.

Rejection of Claims 17-20 Under 35 U.S.C. §103(a), based on *Ooishi et al.* (USP 5,985,712) in view of *Ota et al.*

The invention of amended claim 17 is directed to a semiconductor device having a first region and a second region. In a first region, the semiconductor device includes a first gate electrode having a first lower layer electrode and first upper layer electrode, with a first cap film formed on the first upper layer electrode. In addition, a first nitride film is formed on a side surface of the first upper layer electrode that does not cover a side surface of the first cap film. Similarly, in a second region, the semiconductor device includes a second gate electrode having a second lower layer electrode and second upper layer electrode, with a second cap film formed on the first upper layer electrode. A third nitride film is formed on a side surface of the second upper layer electrode that does not cover a side surface of the second cap film.

To show Applicant's first and third nitride films, the rejection relies on the reference *Ota et al.* *Ota et al.* shows a MOS transistor having a top nitride layer **12B** (argued to correspond to Applicant's cap films). The MOS transistor also includes a gate with a metal layer **50B** (argued to correspond to Applicant's upper layer electrodes) and a polysilicon layer (argued to correspond to Applicant's lower layer electrodes). A nitride spacer **25B** is formed on the sides of the metal layer **50B**, however such a layer covers the side surface of the top nitride layer **12B**:



Thus, because the cited reference does not show or suggest all limitations of claim 17-20, this ground for rejection is traversed.

Amended claim 18 is believed to be separately patentable over the cited combination of references. Claim 18 has been amended to include a thickness limitation of less than 6 nm for the first and third nitride films.

Thus, to address the rejection of claim 18, Applicant incorporates by reference the same general comments set forth above for claim 1. Namely, *Ota et al.* remains silent as to any particular thickness with respect to nitride spacer 25B. Further, the thinness of such a feature is never shown to be a result effective variable, and hence is not obvious.

For all of these reasons this ground for rejection is traversed.

Rejection of Claim 29 Under 35 U.S.C. §103(a), based on *Ooishi et al.* (USP 5,985,712) in view of *Ota et al.*

Claim 29 has been renumbered to claim 28, and depends from claim 27, which depends from claim 21. Claim 29 recited particular limitations aimed at an insulating thickness between contacts and lower gate electrodes of two different transistors.

To address this ground for rejection, Applicant first incorporates by reference the comments set forth above for both claims 1 and 4. Namely, Applicant's second insulating film thickness limitation is neither shown or nor obvious in light of the cited references.

In addition, amended claim 28 includes limitations not shown or suggested any of the cited references.

The rejection appears to admit that Applicant's spacing is not shown in the references, but would be obvious.

> Ota does not disclose a first contact... isolated from the first lower gate electrode by a first insulating thickness; and a second contact... isolated from a second lower gate electrode by a second insulating thickness that is greater than the first insulating thickness. Such contact is conventional to make electrical contact to S/D region as disclosed in Ooishi, fig. 5E. (Office Action, dated 08/25/04, Page 8, Line 20 to Page 9, Line 3.

FIG. 5E from *Ooishi et al.* is shown below. This figure does not support the facts asserted by the rejection. There appears to be no difference in a spacing between a lower gate and contact for the two transistors.

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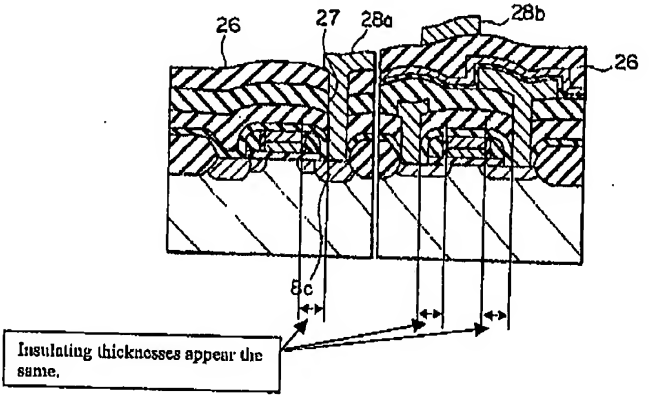

For this reason, the references do not show or suggest the limitations of claim 28, and a prima facie case of obviousness has not been established.

Claims 1, 17-18, 21-22 and 25-29 have been amended. Claims 25-29 have been amended, not in response to the cited art, but to address typographical errors. Claim 4 has been cancelled.

The present claims 1-3, 5-7 and 17-28 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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